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10EC751

Seventh Semester B.E. Degree Examination, Dec.2014/Jan.2015
DSP Algorithms & Architecture

Time: 3 hrs. Max. Marks:100

Note: ***Answer FIVE full questions, selecting at least TWO questions from each part.***

PART – A

1 a. Explain a digital signal processing system with the help of a block diagram. **(07 Marks)**

b. List the major unique architectural features implemented in any programmable DSP devices. **(03 Marks)**

c. Derive the relationship between DFT and frequency response and also define frequency resolution and signal record length. **(06 Marks)**

d. An FFT is employed for determining the frequency components of a random signal. It is required that the resolution of FFT to be <=5 Hz, for a signal with f_{max} = 1.25 kHz. Determine i) Sampling interval, TS.
ii) FFT length (N) as a power of 2.
iii) Minimum signal record length. **(04 Marks)**

2 a. Draw the structure of a 4×4 Braun multiplier and also explain its operation. **(08 Marks)**

b. Explain the pointer updating algorithm for circular addressing mode. **(08 Marks)**

c. Compute the sequence in which the input data should be ordered for a 16 point DIT FFT using Bit reversed addressing mode. **(04 Marks)**

3 a. Describe the following units of TMS320C54XX processor: i) Barrel shifter ii) Central processing unit. **(08 Marks)**

b. What is meant by addressing mode? Explain the absolute, accumulator, direct and indirect addressing modes of TMS320C54XX DSP processor. **(12 Marks)**

4 a. Describe the operation of the following instructions:
i) MAC *AR3-, *AR4+, B, A
ii) MAS *AR3-, *AR+, B, A
iii) RPTZ and RPTB. **(06 Marks)**

b. Explain the hardware timer of TMS320C54XX DSP with logical block diagram. **(07 Marks)**

c. Explain the pipe line operation of TMS320C54XX processor. **(07 Marks)**

PART – B

5 a. What is the significance of Q-notation in DSP? **(04 Marks)**

b. Represent each of the following numbers in desired Q-notation format:
i) -352 as Q_0 number.
ii) 3.125 as Q_7 number.
iii) BDAFh in Q_7 and Q_{15} number.
iv) -0.160123 as Q_{15} number.
v) 4400h as Q_0 number. **(06 Marks)**

c. Explain with the help of block diagram and mathematical equations implementation of decimation filter on TMS320C54XX processor. ***(10 Marks)***

6 a. What minimum size FFT must be used to compute 500 points DFT? What must be done to the samples before the chosen FFT is applied? **(04 Marks)**

b. Derive the optimum scaling factor for the DIT FFT butterfly. **(08 Marks)**

c. Write an assembly language program for implementing following on TMS320C54XX processor:

i) Bit reversed address generation

ii) Spectrum of the transformed data. **(08 Marks)**

7 a. What is an interrupt? With a neat flow chart explain handling of interrupt by TMS320C54XX processor. **(10 Marks)**

b. How does DMA help in increasing the speed of a DSP processor and also explain register sub addressing technique for configuring DMA. **(10 Marks)**

8 a. With neat block diagram explain the DSP based biotelemetry receiver. **(10 Marks)**

b. With neat block diagram explain the CODEC interface circuit. **(10 Marks)**

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